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BOEING

SYNTACTIC VISUAL IMAGE GENERATION SYSTEM
FEASIBILITY STUDY PHASE II
INTERIM FINAL REPORT

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DECEMBER 1982

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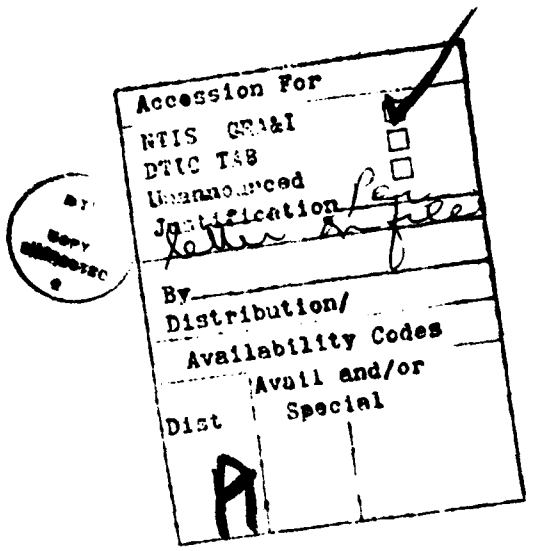

Introduction

This report briefly summarizes the progress of the Syntactic Visual Image Generation program through December 10,1982. A summary of the progress in each subtask will be given, including a discussion of the hardware development status followed by a discussion of the software development status of the program.

General Purpose Equipment Status

A Tektronix 9000 Logic Analyzer with vector stimulator has arrived and is proving to be an effective tool in hardware checkout. The Gould SEL 32/87 computer and the Genisco color raster graphics system have been operating reliably for the past 6 months with little down time due to hardware failures. The Precision Echo EFS-2 color video disc has been delivered and installed. A minor modification to the Genisco graphics system has been completed to permit video recording of scenes to the video disc.

Custom Hardware Status

Figure 1 depicts the latest completed configuration and Figure 2 depicts the next integrated configuration of the architecture research system. The solid lines represent the general purpose equipment configuration, and the dashed lines represent the initial custom hardware. The following discussion outlines the current status of the custom hardware development, including components not occurring in the next configuration.

Frame/Depth Buffer Memory Status

Boeing has completed the design and testing of the intelligent memory for the Architectural CIG System. One module, consisting of one-eigth of the total Depth-Frame Buffer underwent full functional test and was successfully linked to the host computer via a high speed interface located in the test station. Through this interface, Boeing was able to pass pixel data, including depth, color, and screen address to the custom hardware to perform the hidden surface algorithm and output an image to the graphics display. Manufacturing of the remaining seven modules are on schedule.

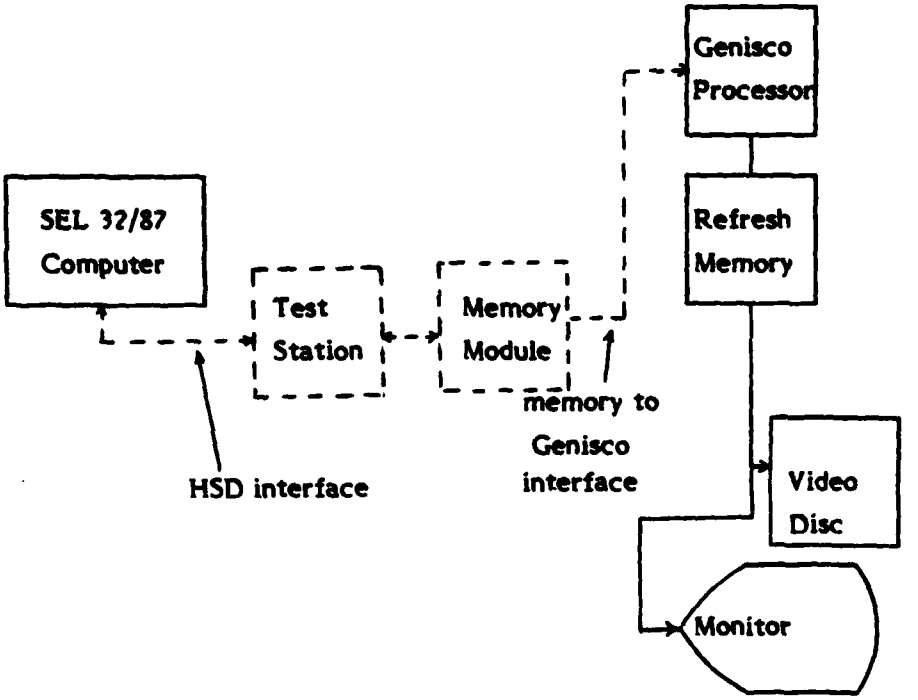

Figure 1 Latest Completed Configuration

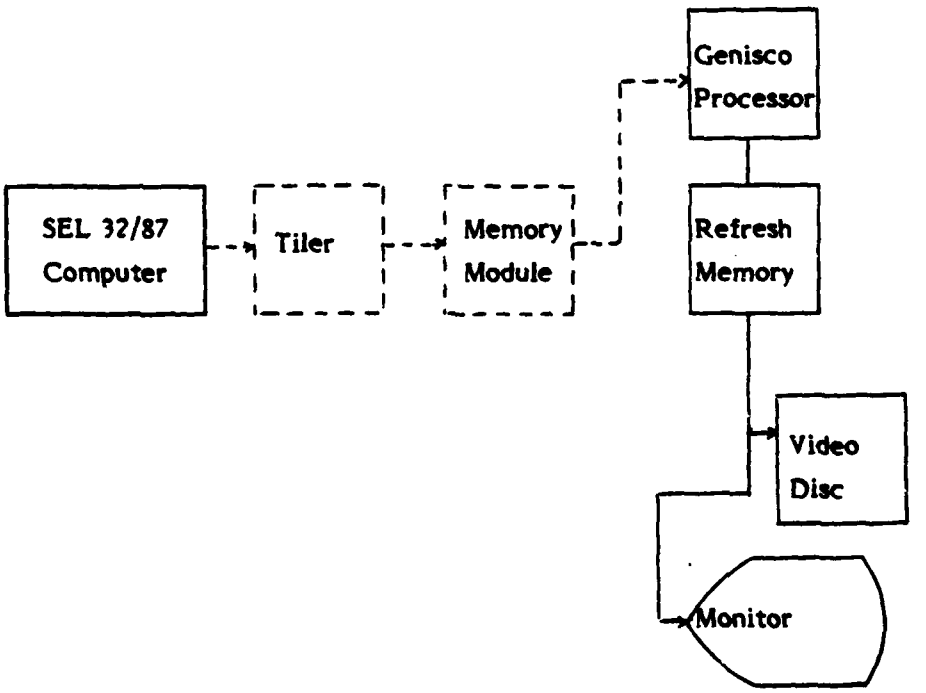

Figure 2 Next Integrated Configuration of Research System

Memory to Genisco Interface Status

As shown in figure 2, the memory to Genisco processor interface circuit is required to route scene data in the custom frame buffer to the display system. This circuit resides on the Anti-Aliaser board which will eventually be expanded to the full operating anti-aliaser. The interface contains 3 modes of memory selection for frame buffer to display screen mapping to test interleaving, scrambling etc. for the eventual full scale research system. The interface board has been designed, fabricated and checked out at the board level. Successful system integration for the board has been completed.

Test Station Development Status

The test station does provide a link between the SEL computer and the various custom boards (memory, tiler, etc.) being developed, so that test and diagnostic software resident in the SEL computer can "stimulate" the custom boards and check for proper response from the boards. The test station contains a SEL computer HSD interface and slots for the various boards to be tested. The test station has been designed, manufactured and successfully checked out. It has been used to check out the tiler and the depth buffer memory.

Splitter Tree Status

The splitter tree, which routes data from tiler to the frame/depth buffer, consists of three levels of switching cells. There are two types of circuit boards and two types of switching cells containing FIFO queues. The first type of circuit containing both types of switching cells, has been manufactured and will undergo checkout beginning in January. The other type of circuit board, containing only one type of switching cell, will be sent to manufacturing after checking out the first circuit board. Work progress is on schedule.

Control/Status Board

The control/status board will be used to control the synchronizing of the CIG execution pipeline and to collect the various CIG statistics from the architecture research system components (e.g. number of triangles tiled data by each tiler). The control status board has been designed, drafted and fabricated. It is on schedule with the checkout in progress.

Tiler Development Status

Each tiler will consist of 2 circuit boards containing a SEL computer HSD interface and 3 major pipelined stages called: (1) Tiling Machine Setup, (2) Tiling Machine, and (3) Tile Accumulate.

Board 1 will contain the HSD interface and the third stage of the tiler (Tile Accumulate). This board has been fabricated and checkout was completed the week of Nov. 1.

Board 2 will contain the first and second stages of the tiler. This board has been fabricated and all manufacturing related problems (ie. wiring errors) have been identified and corrected. Checkout of the two stages (Tiling Maching Setup and Tiling Machine) is 98% complete.

Software Status

Executive and Database Retrieval Software Status

Detailed design of CIG database structure along with executive and database retrieval software is underway. The dataflow charts and data dictionary (design documentation) for this software is 100% complete and designers have begun describing the algorithms in an informal program design language (PDL). In addition code has been created from the PDL and tested for certain modules in the memory management processes.

Object Processor Software Status

Preliminary design of the object processor software for terrain objects and conventional static objects (e.g. buildings, bridges, etc.) has been completed and detailed design is underway. Dataflow charts for these object processors are 100% complete. The design of dynamic objects (e.g. vehicles) software has also been completed, and detailed design is beginning. PDL has been designed for about 75% of the terrain object processor. Coding and testing has begun on this PDL. The static object processor and dynamic object processor have 30% of the PDL and code designed.

Test Station Software Status

The test station software will be resident in the SEL computer and will be used to generate data for testing the custom boards, such as the frame/depth buffer memory, which will be plugged into the test station. Diagnostic software has been developed to execute on the SEL computer and test the memory boards. In addition a tiler driver has been programmed to interface with the tiler through the test station.

Genisco-SEL Interface Software Status

Development of Genisco - SEL interface software has been completed, and scenes are being generated on the SEL computer and successfully displayed by the Genisco graphics system. Scenes can be generated using either a full color (24 bits per pixel) format or a lookup table (8-bit per pixel) format. The HSD handler and routines for using the Genisco have been designed and coded. The Genisco routines are callable from FORTRAN and PASCAL and have been included inn the DARPA SEL 32/87 system library.

Quadric Surface and Stamps Algorithm Development Status

Boeing has developed software to generate scenes using quadric surfaces with Phong shading applied. Boeing has also developed software to apply stamps (digitized scenes of various textures such as bricks) to planar surfaces and to the quadric surfaces. This stamp effort included digitizing color photographs using red, green,

and blue filters of numerous textures (e.g. brick, shingles, cedar siding etc.). Both the curved surface and stamp research was initiated ahead of the original 1983 start dates. The algorithms are not optimal, and further algorithm research and software development in these areas will occur throughout the duration of the program.

Fractal Terrain Algorithm Development Status

Boeing developed software to generate scenes with textured water using a 2-D fractal shading algorithm. The 3-D fractal algorithm used to generate perturbations in elevation and shading of terrain such as snow covered mountains was enhanced to reduce the processing time required by 50%.

Fiscal Status

Total Estimated cost	2,599,681
Total fixed fee	225,597
Expenditures to date	1,520,000
Estimated funds required to complete work	1,079,681
Estimated date of work completion	14 Dec 83